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A Survey Analysis on CMOS Integrated Circuits with Clock-Gated Logic Structure

PADMA KHARE# SHAISTA ANJUM*
LNCT Bhopal, MP, India

Abstract-
Various circuit design techniques has been presented to improve noise tolerance of the proposed CGS logic families. Noise in deep submicron technology limits the reliability and performance of ICs. The ANTE (Average Noise Threshold Energy) metric is used for the analysis of noise tolerance of proposed CGS. A 2-input NAND and NOR gate is designed by the proposed technique. Simulation results for a 2-input NAND gate at clock gated logic show that the proposed noise tolerant circuit achieves 1.79X ANTE improvement along with the reduction in leakage power. Continuous scaling of technology towards the manometer range significantly increases leakage current level and the effect of noise. This research can be further extended for performance optimization in terms of power, speed, area and noise immunity.
Keywords— Static CMOS Logic, Domino Logic, Feed through Logic (CGS), Low Power.

I. INTRODUCTION

In the fast growing VLSI industry transistor density per chip is increasing day by day following the Moore's law.With increase in transistor density, area and power consumption also increases. The design engineers are striving to achieve more and more functionality at higher speed and low power, keeping area and cost low. Circuit design techniques also plays an important role in achieving high performance, low power or low area. Design engineers can consider different logic design techniques according to the need of their design. Some designs need to be very fast despite of area and power dissipation, example in some real time systems, while some requires very low power and small area, as in like portable devices. In this paper different logic design techniques are discussed and a comparative analysis has been done between them for power and speed. All the design techniques have their own characteristics, advantages and drawbacks. For example in static CMOS circuits power dissipation is low but are very slow and implementation area is large as compared to domino. On the other hand dynamic logic circuits are very fast and have low area but dissipate more dynamic power as compared to static CMOS logic. There are some other proposed techniques such as feedthrough logic (FTL) and low power CGS which further improves the characteristics of domino logic and also solves many problems of domino logic such as non inverting logic, use of inverter at the output and charge sharing etc. One another proposed technique called zigzag keeper is also discussed here which reduces the power dissipation largely but at the cost of area overhead. At last, between these techniques a comparative analysis has been done based on literature survey and previous papers, so that to make it easy to select from these different techniques according to the need.

II. STATIC CMOS LOGIC

Static CMOS logic is the most commonly used logic design technique. In this circuit are made up of two networks namely pull up network (PUN) and pull down network (PDN) (Fig. 1). PUN consists of PMOS transistors and PDN consists of NMOS transistors. Input to these networks is dual of each other. Output is connected to power supply or ground based on the inputs applied to PUN and PDN making the output 1 or 0 respectively.
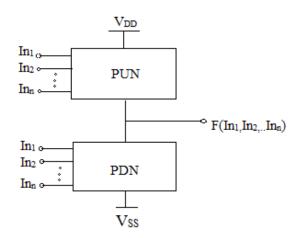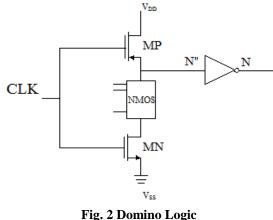

Fig. 1 Static CMOS Logic

One of the advantages of Static CMOS circuits is that they have high noise margin so they are more scalable than dynamic logic. Therefore threshold voltage of transistors can be lower than dynamic logic circuits. So performance of circuits can be improved which are designed for ultra low voltage . In steady state mode there is no direct path between VDD and ground so power dissipation is only due to leakage current in transistors. The main drawback of static CMOS logic is that it uses more number of PMOS transistors which increases the delay and area of the circuit. To design a logic gate with n inputs, 2n transistors are required which results in large area of the circuit. And in some logic implementations PMOS transistors occurs in series due to which input capacitances increases and the output driving capability of the circuit reduces . Also in these circuits in some logic implementations, different paths have different delays, so glitches or spurious transitions can occur . For large fan-in gates performance of this logic family is not very good.

III. DOMINO LOGIC

Domino logic design technique is the improved version of dynamic logic family. Fig. 2 shows domino logic which consists of a dynamic logic circuit followed by a static CMOS inverter. This circuit consists of a PMOS pre-charge transistor MP and an NMOS evaluation transistor MN with their gates connected to clock, and there is an NMOS logic network which implements the required logic function. During the pre-charge phase (Clock = 0) the output of the circuit get charged through the pre-charge transistor MP to the level of VDD and the output of inverter is low. Now during the evaluation phase (Clock = 1) the evaluation transistor MN is ON, and the output of the dynamic circuit either discharges to ground or remains at high level depending on the inputs applied to the NMOS network.

Fig. 2 Domino Logic

In circuits of domino logic there can be other capacitive nodes in NMOS block which shares the charge of the output node capacitance, which decreases the output voltage level, this problem is called charge sharing.

One of the major advantages of the domino logic over the static CMOS is that this works on high frequency clock and there is no PUN so this eliminates the spurious transitions and corresponding power dissipation. But in some logical conditions output is pre-charged only to discharge in the evaluation phase, for example, if output is low and we apply inputs which gives low output then in pre-charge phase the output will charge to high voltage and during evaluation phase it will discharge to low, increasing the power dissipation. Therefore, the signal activity increases for this circuit design technique and this increased signal activity along with the extra load that the clock line has to derive are the main reasons for high power dissipation in domino logic as compared to static CMOS circuits. Noise margin of Domino logic circuits is low as compared to static CMOS circuits so they are not as scalable as static CMOS. So transistor threshold voltage is kept high to reduce leakage in domino logic circuits. As compared to static CMOS area is reduced in domino logic circuits because of the reduced number of PMOS transistors. Also there is no short circuit power dissipation in domino and they have strong output driving capability .

IV. PROPOSED METHODOLOGY

In this paper work, the proposed clock gated logic has been studied. Clock-gated logic is shown in fig. 3. This logic circuit consists of a PMOS load transistor Mp and an NMOS reset transistor Mr and an NMOS block in which inputs are applied. The gates of the load transistor and the reset transistor are connected to clock. When clock =1(reset phase) load transistor Mp is OFF and reset transistor Mr is ON and the output is reset to logic low. Now when clock =0(evaluation phase) load transistor Mp is ON and reset transistor Mr is OFF and the output either goes to logic level high or remains at low logic according to the inputs applied to the NMOS block. So in this output can either go from 0 to 1 or remain at 0 level according to the applied inputs.
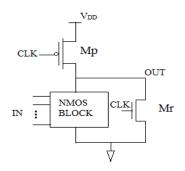

Fig. 3 Clock-gated Logic

In CGS the output logic level is evaluated before all the inputs are valid, so its speed is very high. The problems in domino logic circuits like charge sharing and use of inverter at the output are also solved. In domino logic an inverter is needed at the output during cascading and the output is charged to VDD so there is high dynamic power dissipation but in CGS output is reset to low before evaluation during reset phase eliminating the requirement of inverter for cascading. The performance analysis of a chain of 10 inverters using CGS in shows that when clock =1 the output of each stage goes to logic 0 and when clock =0, voltage at the output node of the cascaded gate rises to threshold voltage of the gate and then if input changes, the output makes transition from threshold voltage to high level or low level. So in this as transition is from threshold voltage to high or low level, the speed is increased to a greater extent. But in this logic there is more power dissipation because minimum output low voltage is not 0V. Noise margin is reduced in CGS

A. Low power proposed modified CGS (LP-CGS)

The proposed modified circuit is shown in Fig. 4(a). This circuit reduces VOL by using one additional PMOS transistor MP2 in series with MPL The operation of this circuit is similar to that of CGS in. During reset phase i.e. when CLK = 1, output node is pulled to ground (GND) through M, During evaluation phase output node charges through MpJ and Mp2 When CLK goes low (evaluation phase) Mr is turned off and the output node conditionally evaluates to logic high (V OH) or low (VOL) depending upon input to NMOS block. If the NMOS block evaluates to high then output node pulled toward V DD i.e. V OH =V DD, otherwise it remain at logic low i.e. VOL. Since MpJ and Mp2 are in series the voltage at drain of MpJ is less than V DD. During evaluation due to ratio logic the output node pulled to logic low voltage i.e. VOL which is less than the V OL of existing CGS. This reduction in VOL causes significant reduction in dynamic power consumption but due to the insertion of PMOS transistor Mp2 propagation delay of the proposed LP-CGS in Fig. 4(a). Increases. The propagation delay of propose CGS circuit can be improved by using an NMOS transistor as shown in Fig. 4(b).

B. High speed proposed modified CGS (HS-CGS)

In order to improve the speed of proposed LP-CGS structure the reset transistor Mr is connected to V DDI2 as shown in Fig. 4(b). The operation of this circuit is as follows, when CLK =1, the output node (OUT) will charges to the threshold voltage Vm During evaluation phase

according to input value the output node only makes partial transition from V TH to V OH or VOL. Since during evaluation phase the output node (OUT) only makes partial transitions, this improves propagation delay. An inverter designed by using HS-CGS is shown in Fig 4(c).
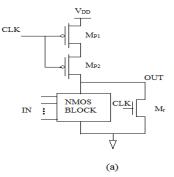

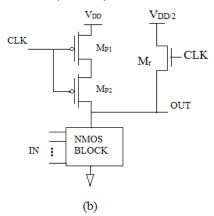**Fig. 4. (a) Proposed modified low power CGS structure (LP-CGS).**

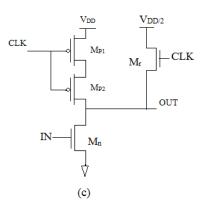**Fig 4(b) Proposed modified high speed CGS structure   (HS-CGS).**

Fig 4(c) Circuit diagram of inverter using HS-CGS structure

Logic family	Power (µW)	t_p (ns)	PDP (µW*ns)
FTL	290.1	1.294	375.38
Proposed LP-FTL	183.2	1.743	319.31
Proposed HS-FTL	316.9	0.95	301.05

V. CONCLUSION

In this paper we find out the low power dynamic circuit. The proposed circuit was simulated in clock gated technology using EDA tool. The simulation for a long chain of inverter (10-stage) and S-bit ripple carry adder can also carried out in this work. The proposed modified circuits can be used for design of various low-power or high performance logic circuits as per requirement. We will focus on implementing this logic circuits into efficient memory block using registers made up of latches and flip-flops.

REFERENCES

[1.] S .Mathew, M. Anders, R.Krishnamurthy, S. Borkar, "*A 4 GHz 130 nm address generation unit with 32-bit sparse-tree adder core*," IEEE VLSI Circuits Symp. , Honolulu, Hi,jun 2002, pp. 126-127.

[2.] S. vangal, Y. Hoskote, D. Somasekhar, V. Erraguntla, J. Howard, G.Ruhl, V. Veeramachaneni, D. Finan, S. Mathew, and N. Borkar, "*A 5-GHz floating point multiply-accumulator in 90-nm dual VT CMOS*," in Proc. iEEE Int. Solid-State Circuits Conf, San Francisco, CA, Feb.2003, pp. 334-335.

[3.] R.K. Krishnamurthy, S. Hsu, M. Anders, B. Bloechel, B. Chatterjee, M. Sachdev, S. Borkar, "*Dual Supply voltage clocking for 5GHz 130nm integer execution core*," proceedings of IEEE VLSI Circuits Symposium, Honolulu Jun. 2002, pp. 128-129.

[4.] V. Navarro-Botello, J. A. Montiel-Nelson, and S. Nooshabadi, " *Analysis of high performance fast clock-gated logic families in CMOS*," iEEE Trans. Cir. & syst. ii, vol. 54, no. 6, Jun. 2007, pp .489-493

[5.] Y.jiang, A. A1-sheraidah, Y. Wang, E.sha, J. Chung, A novel Multiplexer based low-power full adder, IEEE Trans. Circuits Syst.lI, vol. 52,2004, pp. 345-348.

[6.] J.M. Rabaey, A. Chandrakasan, B. Nikolic, 'Digital Integrated Circuits: A Design perspective' 2e Prentice-Hall, Upper saddle River, NJ, 2002.

[7.] S. M. Kang, Y. Leblebici, 'CMOS Digital Integrated Circuits: Analysis & Design', TATA McGraw- Hill Publication, 3e, 2003.

[8.] N. Weste, K. Eshraghian, 'Principles of CMOS VLSI Design, A systems perspective', Addision Wesley MA,1988.

[9.] K.S. Yeo, K. Roy, 'Low- Voltage, Low-Power VLSI Subsystems'.

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